Docket No.: M4065.0159/P159-A
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Li Li, et al.

Application No.: Not Yet Assigned

Group Art Unit: 2815

Filed: July 12, 2001

Examiner: P. Brock

For: METHOD OF CONTROLLING SRIATIONS AND CD LOSS IN CONTACT OXIDE ETCH

PRELIMINARY AMENDMENT

Box Non-Fee Amendment
Commissioner for Patents
Washington, DC 20231

Dear Sir:

Prior to examination on the merits, please amend the above-identified U.S. patent application as follows:

In the Specification

Page 1, after the title, please insert – This application is a divisional of application Ser. No. 09/292,393, filed on April 15, 1999, which is hereby incorporated by reference.—

Rewrite paragraphs 0007, 0008, 0009, 0036, and 0038 as follows:

In the Claims

Please cancel claims 1-58 and 85-91.

1317658 v1, S8PM01! DOC

Replacement Paragraphs

[0007] During photolithography, problems arise because high resolution submicrometer images in photoresist require shallow depth of focus during exposure, but thick photoresist patterns are required because of the poor etch rate between the photoresist and the underlying semiconductor layer. Additional problems occur because of the uncontrolled bake during the plasma etch processing. During this process, the substrate is exposed to ion and electron bombardment, UV light, X-rays, and scattered radiations. As a consequence, irregular topographies, distorted images and CD loss occurs during the exposure of the photoresist layer as shown in Figs. 1-2. These figures illustrate a typical plasma etch of a silicon substrate 40 having an oxide layer 42 deposited thereon. Contact holes 12, 14, 16 are etched into wafer 10. The contact holes 12, 14, 16 have an upper surface 38 and a lower surface 36. Due, in part, to the thin DUV resist and the uncontrolled bake during the etching process, discontinuities 18, 20, 22, 24, 26, 28, 30 and 46 are formed as shown for contact hole 12. The discontinuities 18, 20, 22, 24, 26, 28, 30, 46 occur in the contact hole 12 as a result of the plasma etch attacking the side walls of the contact hole 12. It should be understood that the shape and number of the discontinuities will vary depending upon the specific etching process parameters as well as the material which is being etched. The discontinuities may form which have a first surface 32 and a second surface 34 in the wall 44 of the contact hole 12. In addition, contact holes 12, 14, 16 are formed in a frusto-conical shape instead of a cylindrical shape when formed in the oxide layer 42.

[0008] When two discontinuities 22, 46 are formed in adjacent contact holes 12, 14 and become aligned with one another, the integrated circuit suffers a loss in critical dimension (CD loss). CD loss is a critical component of integrated circuit design, especially in the sub-quarter micron regime. Additionally, when the contact holes 12, 14, 16 are formed in a frusto-conical shape instead of the desired cylindrical shape, surface area is sacrificed thereby requiring the contact holes 12, 14, 16 to be deeper to effectuate the same contact.

[0009] A further problem with the prior plasma etching is that as a result of the irregular contact holes 12, 14, 16, an unwanted and uncontrolled increase in the diameter of the contact holes 12, 14, 16 may also result. This increased size also impacts the displacement of the metal atoms that fill the contact holes. Thus, in addition to the loss in critical dimension, electrical contacts may also become unreliable.

[0036] The plasma etching gas may be any gaseous material known for etching. Examples of suitable plasma etching gases are those such as HBr, Cl, fluorocarbon containing gases and the like. It should be understood that the selection of the plasma etching gas will be determined by the substrate to be etched as well as the physical parameters of the etching process such as power, pressure, temperature and the like. Examples of some preferred gases for use with the present invention include: HBr, Cl_2 carbon tetrafluoride (CF_4) trifluoromethane (CHF3) and the like. The low power plasma is formed at low power, such as, for example, 100 to about 250 watts (RF), preferebly about 150 watts.

[0038] Reference is now made to Fig. 8. The substrate 116 is then etched out by a directional etching process such as reactive ion etching. Etching is continued down to the level of the substrate to form a set of trenches 132, 134, 136. The plasma etching is carried out under ordinary high power etching conditions. The plasma etch may be formed at a power of from about 800 to about 1100 watts (RF), preferably at from about 950 watts. Any suitable etching gas may be used in accordance with the present invention. Preferably, the same etching gases used in the low power plasma etching step are used in the high power plasma etching. In fact, it is an advantage of the present invention that the plasma etching parameters, such as gas composition, reactor pressure and the like do not need to be modified. This allows the present invention to efficiently etch the substrate 116 without the need for additional time consuming processing steps. The substrate can be contacted with the high power etch for any time sufficient to etch the underlying substrate. It should be understood that these times may vary from about 30 seconds to over 500 seconds, depending upon the substrate, the etching gas and the

physical parameters of the plasma etch. The additional photoresist 120 is then removed from the substrate 116 to arrive at the device shown in Fig. 9.

REMARKS/ARGUMENTS

The specification has been amended to include a reference to prior application Ser. No. 09/292,393 filed on April 15, 1999, as required by 37 CFR 1.78(a)(2). Also changes in the specification were made to correct minor labeling errors in the parent application.

Claims 1-58 and 85-91 have been canceled. The pending application now contains claims 59-84.

Allowance of the application is solicited.

Dated: July 12, 2001

Respectfully submitted,

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Version with Markings to Show Changes Made to Specification

Paragraphs 0007, 0008, 0009, 0036 and 0038 have been amended as follows:

[0007] (Amended) During photolithography, problems arise because high resolution submicrometer images in photoresist require shallow depth of focus during exposure, but thick photoresist patterns are required because of the poor etch rate between the photoresist and the underlying semiconductor layer. Additional problems occur because of the uncontrolled bake during the plasma etch processing. During this process, the substrate is exposed to ion and electron bombardment, UV light, X-rays, and scattered radiations. As a consequence, irregular topographies, distorted images and CD loss occurs during the exposure of the photoresist layer as shown in Figs. 1-2. These figures illustrate a typical plasma etch of a silicon substrate 40 having an oxide layer 42 deposited thereon. Contact holes [10, 12, 14] 12, 14,16 are etched into wafer 10. The contact holes [10, 12, 14] 12, 14, 16 have an upper surface 38 and a lower surface 36. Due, in part, to the thin DUV resist and the uncontrolled bake during the etching process, discontinuities 18, 20, 22, 24, 26, 28, 30 and 46 are formed as shown for contact hole [10] 12. The discontinuities 18, 20, 22, 24, 26, 28, 30, 46 occur in the contact hole 12[, 14] as a result of the plasma etch attacking the side walls of the contact [holes 12, 14] hole 12. It should be understood that the shape and number of the discontinuities will vary depending upon the specific etching process parameters as well as the material which is being etched. The discontinuities may form which have a first surface 32 and a second surface 34 in the wall 44 of the contact hole 12. In addition, contact holes [10, 12, 14] 12, 14, 16 are formed in a frusto-conical shape instead of a cylindrical shape when formed in the oxide layer 42.

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desired cylindrical shape, surface area is sacrificed thereby requiring the contact holes [10, 12, 14] 12, 14, 16 to be deeper to effectuate the same contact.

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[0036] (Amended) The plasma etching gas may be any gaseous material known for etching. Examples of suitable plasma etching gases are those such as HBr, Cl, fluorocarbon containing gases and the like. It should be understood that the selection of the plasma etching gas will be determined by the substrate [to the] to be etched as well as the physical parameters of the etching process such as power, pressure, temperature and the like. Examples of some preferred gases for use with the present invention include: HBr, Cl_2 carbon tetrafluoride (CF_4) trifluoromethane (CHF3) and the like. The low power plasma is formed at low power, such as, for example, 100 to about 250 watts (RF), preferably about 150 watts.

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time consuming processing steps. The substrate can be contacted with the high power etch for any time sufficient to etch the underlying substrate. It should be understood that these times may vary from about [30seconds] 30 seconds to over 500 seconds, depending upon the substrate, the etching gas and the physical parameters of the plasma etch. The additional photoresist 120 is then removed from the substrate 116 to arrive at the device shown in Fig. 9.